

326	32	Subclass
ISSUE CLASSIFICATION		

PATENT NUMBER

U.S. REISSUE Patent Application

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10-2 Q.A.

1-29-02

APPLICATION NO. 09/963735	CONT/PRIOR D F	CLASS 326	SUBCLASS 39	ART UNIT 2819	EXAMINER D Le
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APPLICANTS:

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Semiconductor integrated circuit with mixed gate array and standard cell

PTO-2040
12/89

☒ SURRENDER OF ORIGINAL PATENT

(Exr. initials)

ORIGINAL PATENT NUMBER 6054,842

ISSUING CLASSIFICATION

[illegible]

<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg. <u>17</u>	Figs. Drwg. <u>18</u>	Print Fig. <u>3A</u>	Total Claims <u>65</u>	Print Claim for O.G. <u>30</u>
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner) _____ (Date)			NOTICE OF ALLOWANCE MAILED	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S. Patent. No. _____	DON LE PRIMARY EXAMINER <u>X</u> <u>le</u> <u>5/7/83</u> (Primary Examiner) (Date)			ISSUE FEE	
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.				Amount Due	Date Paid
FINAL SPRE REVIEW _____ (INITIALS)	_____ (Legal Instruments Examiner) _____ (Date)			ISSUE BATCH NUMBER	

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